In the Claims

Applicant has submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. Claims 1 and 5 have been amended.

1. (Currently amended) A memory cell, ~~comprising~~consisting essentially of:

a charge storage element;

a one-transistor switch constructed and arranged to selectively connect the storage element to a first data line, responsive to a first select signal; and

a one-transistor gain element having an input connected to receive a signal from the storage element and constructed and arranged to selectively provide a corresponding output signal to a second data line, responsive to a second select signal, the gain element ~~comprising~~consisting essentially of a FET having a first terminal connected to the storage element, a second terminal connected to the second data line and a third terminal selectively connected to one of a first power supply and a second power supply, the FET being symmetrical with respect to the second and third terminals.

2. Canceled

3. Canceled

4. (Previously presented) The memory cell of claim 1, wherein the switch transfers a signal from the first data line onto the storage element and transfers a signal from the storage element onto the first data line when selected by the first select signal.

5. (Currently amended) A two-dimensional array of memory cells, comprising:

a first select signal line running through the array in a first direction;

a second select signal line running though the array in a second direction;

first and second data lines; and

each cell having

a charge storage element,

a one-transistor switch constructed and arranged to selectively connect the storage element to the first data line responsive to a first select signal, and

a one-transistor gain element having an input connected to receive a signal from the storage element and constructed and arranged to selectively provide a corresponding output signal to a second data line, responsive to a second select signal, the gain element ~~comprising~~consisting essentially of a FET having a first terminal connected to the storage element, a second terminal connected to the second data line and a third terminal selectively connected to one of a first power supply and a second power supply.

6. (Original) A method of addressing an array of memory cells, comprising:

writing groups of bits linearly arrayed with respect to each other; and

reading groups of bits linearly arrayed with respect to each other and orthogonally disposed to the groups of bits written.

7. (Previously presented) The memory cell of claim 1, wherein the first terminal is a gate, the second terminal is a source and the third terminal is a drain.

8. (Previously presented) The memory cell of claim 5, wherein the FET is symmetrical with respect to the second and third terminals.

9. (Previously presented) The memory cell of claim 8, wherein the first terminal is a gate, the second terminal is a source and the third terminal is a drain.

10. (Previously presented) The memory cell of claim 1, wherein the switch transfers a signal from the first data line onto the storage element and transfers a signal from the storage element onto the first data line when selected by the select signal.

11. (Previously presented) A memory cell, consisting essentially of:

a charge storage element;

a one-transistor switch constructed and arranged to selectively connect the storage element to a first data line, responsive to a first select signal; and

a one-transistor gain element having an input connected to receive a signal from the storage element and constructed and arranged to selectively provide a corresponding output signal to a second data line, responsive to a second select signal, the gain element comprising a FET having a first terminal connected to the storage element, a second terminal connected to the second data line and a third terminal selectively connected to one of a first power supply and a second power supply, the FET being symmetrical with respect to the second and third terminals.

12. (Previously presented) The memory cell of claim 11, wherein the FET is symmetrical with respect to the second and third terminals.

13. (Previously presented) The memory cell of claim 12, wherein the first terminal is a gate, the second terminal is a source and the third terminal is a drain.